

**B.L.D.E.A's**  
**S.B.Arts and K.C.P Science College, Vijayapur.**  
**M.Sc.(CS) Programme**



**Student Seminar**

**Sub: Computer System Architecture**

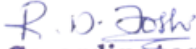
**Date: 19/01/2022**

**Conducted By:**  
**Prof.(Smt) R.D.Joshi**

**B.L.D.E.A's**  
**S.B.Arts and K.C.P Science College, Vijayapur.**  
**M.Sc(CS) Programme**

## **NOTICE**

**All the I semester students are hereby informed to attend the Seminar on "Computer System Architecture - Implemetation of FULL ADDER & HALF ADDER ". Date :19/01/2022 at 9:00 am in Lecture Hall 1.**

  
**Co-ordinātor**  
M.Sc. (C.S.) Programme  
S.B.Arts & K.C.P.Science College,  
Vijayapur.

  
**IQAC, Co-ordinator**  
S.B.Arts & K.C.P.Science College,  
Vijayapur.

  
**Principal**  
S.B.Arts & K.C.P.Science College,  
Vijayapur.

## **A Report on**

A session on seminar was conducted on the 19/01/2022 at the Classroom, M.Sc(CS) Programme. The main intention to conduct a Class Seminar is to encourage the students and to observe their presentation skills and communication skills, ability to present on the given subject. Also to guide them to improvement in taking part in seminar and Conferences.

Mr Veerabhadrayya Hiremath gave seminar on “Implemetation of FULL ADDER & HALF ADDER ”. He explained it with diagrammatic representation and also with table and K-Map.

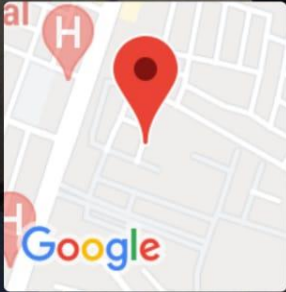
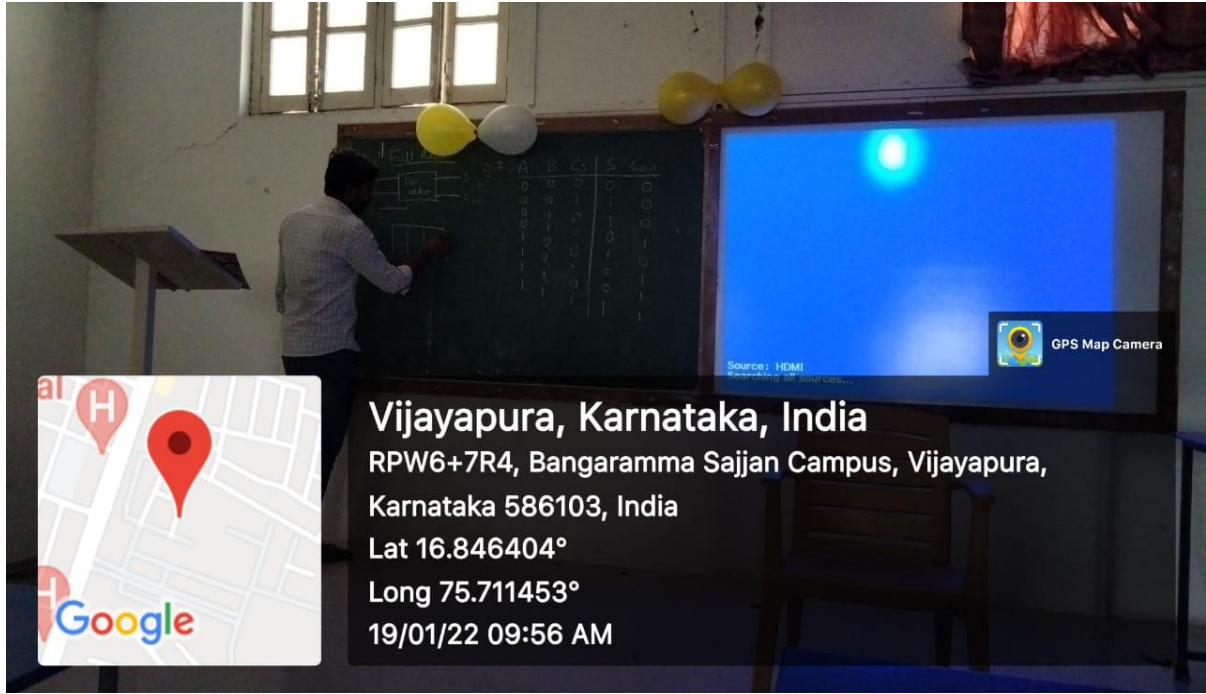
At the end of the seminar there was a time to clear the doubts regarding topic.



*R. D. Joshi*  
**Co-ordinator**  
M.Sc. (C.S.) Programme  
S.B.Arts & K.C.P.Science College,  
Vijayapur.

*[Signature]*  
**IQAC, Co-ordinator**  
S.B.Arts & K.C.P.Science College,  
Vijayapur.

*[Signature]*  
**Principal**  
S.B.Arts & K.C.P.Science College,  
Vijayapur.



## Vijayapura, Karnataka, India

RPW6+7R4, Bangaramma Sajjan Campus, Vijayapura,  
Karnataka 586103, India

Lat 16.846404°

Long 75.711453°

19/01/22 09:56 AM